

**GOVT. POLYTECHNIC KENDRAPARA****LESSON PLAN****Session(2024-2025)**

<b>Discipline:</b> Electronics & Telecommunication Engineering	<b>Semester:</b> 5 <sup>th</sup> , Winter/2024	<b>Name of the Faculty:</b> JOGESWAR NAIK(LECTURER)
<b>Subject:</b> VLSI & Embedded System, Theory-2	<b>No. of Days/week:</b> 04	<b>Start Date:</b> 01/07/2024 <b>End Date:</b> 08/11/2024

<b>Week</b>	<b>Class Day</b>	<b>Theory Topics</b>
1st week 1st july to 6th july	1st	<b>Unit-1: Introduction to VLSI &amp; MOS Transistor, Historical</b>
	2nd	Classification of CMOS digital circuit types
	3rd	Introduction to MOS Transistor & Basic operation of
	4th	Structure and operation of MOSFET (n-MOS enhancement type) &
2nd week 08th july to 13th july	1st	MOSFET V-I characteristics, Working of MOSFET
	2nd	Modeling of MOS Transistors including Basic concept the SPICE level-1
	3rd	Flow Circuit design procedures
	4th	VLSI Design Flow & Y chart
3rd week 15th july to 20th july	1st	Design Hierarchy, VLSI design styles-FPGA.
	2nd	Gate Array Design, Standard cells based design, Full custom
	3rd	Revision
	4th	Quiz
4th week 22nd july to 27th july	1st	<b>Unit-2: Fabrication of MOSFET, Simplified process sequence for fabrication</b>
	2nd	Basic steps in Fabrication processes Flow
	3rd	Fabrication process of nMOS Transistor
	4th	CMOS n-well Fabrication Process Flow
5th week 29july to 3rd august	1st	MOS Fabrication process by n-well on p-substrate
	2nd	CMOS Fabrication process by P-well on n-substrate
	3rd	Layout Design rules
	4th	Stick Diagrams of CMOS inverter
1st week 5th august to	1st	Revision
	2nd	Quiz

28th Oct

	3rd	VLSI, Semi-Custom ASIC (Gate Array & Standard Cell)
	4th	PLD (Programmable Logic Device)
1st week 2nd Nov to 8th Nov	1st	PLD (Programmable Logic Device)
	2nd	Basic idea of Arduino micro controller
	3rd	Basic idea of Arduino micro controller
	4th	Revision

